General Guidelines & Procedures for Using the HMC661LC4B with an Analog-to-Digital Converter

1.0 Introduction

Wideband data acquisition systems with multi-GHz bandwidth are needed for a variety of applications such as software defined radio, radar systems, electronic warfare (EW)/electronic intelligence (ELINT), and test and measurement equipment. Ideally, system designers would like to be able to connect the signal source (for example an antenna) directly to a wideband, high dynamic range Analog-to-Digital Converter (ADC) for digitization. Many of these applications involve sub-sampling where the signal of interest is a high frequency signal well beyond the ADC sample rate. A key limitation to this approach is that current ADCs do not usually have sufficient bandwidth for these very wideband applications. Although several high speed ADCs offer enhanced sample rates, few of them offer input bandwidth beyond a few GHz. In addition, maintenance of good sampling linearity at frequencies above the UHF band is technologically challenging and most current ADCs suffer rapidly degrading linearity above 1 or 2 GHz signal frequency.

These limitations can be overcome using the HMC661LC4B Ultra Wideband Track-and-Hold Amplifier (THA) which is designed for use in microwave data conversion applications requiring maximum sampling bandwidth, high linearity over a wide bandwidth, and low noise. The HMC661LC4B, which offers 18 GHz input bandwidth and excellent broadband linearity, is used as an external master sampler at the front end of the ADC. Once extended-bandwidth sampling takes place within the HMC661LC4B, the low bandwidth held output waveform can by processed by an ADC with substantially reduced bandwidth. ADC linearity limitations at high input frequencies are also mitigated because the settled THA waveform is processed with the optimal baseband linearity of the ADC. Additionally, the HMC661LC4B offers very low random sample jitter of <70 fs which minimizes jitter induced signal-to-noise (S/N) ratio degradation at high microwave signal frequencies. This jitter is significantly better than that typically obtained from currently available ADCs. The result is a radical extension in input bandwidth, substantial improvement in high frequency linearity, and improved high frequency S/N ratio for the THA-ADC assembly compared to the performance of the ADC alone.

This application note provides guidelines for using the HMC661LC4B with high speed ADCs to enhance their bandwidth and high frequency performance. An overview of THA operation and general operating recommendations for maximizing device performance are described. The setup and timing adjustment of a typical evaluation board - based breadboard assembly incorporating the HMC661LC4B as a master sampler for high speed ADCs is also provided. Examples of the performance that can be obtained when the HMC661LC4B is used in an evaluation board setup with some current high speed ADCs may be found in the companion Hittite application note: *Bandwidth & Performance Improvements of High Speed A/D Converters Using the HMC661LC4B*.

2.0 HMC661LC4B Track-and-Hold Amplifier Description & Operation

2.1 HMC661LC4B Track-and-Hold Amplifier General Description

Hittite's HMC661LC4B is a single rank 18 GHz, Track-and-Hold Amplifier optimized for use in microwave data conversion applications requiring maximum sampling bandwidth, high linearity over a very wide bandwidth, and low noise. A single THA produces an output which consists of two time segments. In the track mode interval of the output waveform (positive differential clock voltage for the HMC661LC4B), the device behaves as a unity gain amplifier which replicates the input signal at the output, subject to the input bandwidth and the output amplifier bandwidth limitations. At the positive-to-negative clock transition the device samples the input signal with a very narrow sampling time aperture and holds the output relatively constant during the negative clock interval at a value which is representative of the signal at the instant of sampling.

Table 1 summarizes some of the key performance parameters of the HMC661LC4B. Unlike other available high speed THAs, which suffer substantial bandwidth degradation at full scale input levels, the HMC661LC4B provides 18 GHz sampling bandwidth over the full range of input level up to a full scale differential input of 1 Vp-p and up to 4 GS/s sampling rate. The THA maintains excellent linearity over a very broad bandwidth with 56 dB or

better Spurious Free Dynamic Range (SFDR) from DC to >5 GHz at full scale input. An important feature of the HMC661LC4B is that it exhibits proper linearity order dependence (a 6 dB reduction in input level results in 12 dB and 18 dB reduction in 2nd and 3rd order harmonic product levels respectively). This is particularly important for designers who are employing signal averaging using Digital Signal Processing (DSP). These users may perform post conversion processing to reduce the wideband noise floor and may choose to tradeoff input signal level for higher linearity. As Table 1 shows, a reduction of input level to half-full scale results in 10-bit or better linearity across a wide bandwidth.

Table 1. HMC661LC4B Performance Summary

Parameter	Typ.	Units
Input Sampling BW (THA Mode)	18	GHz
Gain	1	V/V
Maximum Sampling Rate	4	GS/s
Full Scale Differential Input Level	1	Vp-p
Single Tone SFDR (Fin = 1 GHz) [1]	56 / 67	dB
Single Tone SFDR (Fin = 2 GHz) [1]	56 / 65	dB
Single Tone SFDR (Fin = 4 GHz) [1]	57 / 68	dB
Single Tone SFDR (Fin = 8 GHz) [1]	43 / 55	dB
Sampling Aperture Jitter	< 70	fs
Hold-mode Sample Output Noise [2]	1.05	mV rms
DC Power Dissipation	1.59	W

[1] Clock rate = 1 GHz, input signal @ full scale/half-full scale level
[2] Measured with no output filtering (On-chip output amplifier bandwidth approximately 7 GHz)

The HMC661LC4B provides DC-coupled, differential signal I/O and differential clock inputs. All inputs and outputs are 50 Ohm impedance for each differential half-circuit and they operate at true ground-referenced common-mode potential. The HMC661LC4B is housed in a RoHS compliant 4 x 4 mm QFN leadless ceramic package. The HMC661LC4B is ideal for software defined radio, military and commercial radar systems, EW and ELINT systems applications. The HMC661LC4B can also be utilized for spread spectrum processing, wideband spectrum analysis, and high speed digital and analog test instruments including digital sampling oscilloscopes.

2.2   HMC661LC4B General Operating Recommendations

Please refer to the HMC661LC4B product data sheet for complete details. Some key operating notes are summarized here for the reader's convenience.

Power Supply Sequencing

The recommended power supply startup sequence is VccOB, VccOF, VccTH, VccCLK, Vee / VeeCLK if biased from independent supplies. VccOB, VccOF, VccTH and VccCLK can be connected to one +2 V supply if desired.

Input Signal Drive

For best results, the inputs should be driven differentially. The input can be driven single-ended but the linearity of the device will be degraded somewhat. The unused input should be terminated in 50 Ohms when driving the device single-ended.

Clock Input

The device is in track-mode when (CLKP - CLKN) is high and it is in hold-mode when (CLKP – CLKN) is low. The clock inputs should be driven differentially if possible. The clock inputs can be driven single-ended if desired but the single-ended amplitude/slew rate should be similar to the full differential amplitude / slew rate recommended for differential drive. The unused input should be terminated in 50 Ohms.

The T/H-mode linearity of the device varies somewhat with clock power at lower clock frequencies as shown in the performance data plots. This results from a weak dependence of the linearity on clock zero crossing slew rate for slew rates beneath a critical value. For optimal linearity and jitter, a clock zero-crossing slew rate of roughly 2 - 4 V/ns (per clock input) or more is recommended.

For sinusoidal clock inputs, 4 V/ns corresponds to a sinusoidal clock power per differential half-circuit input of -6 dBm at 4 GHz, 0 dBm at 2 GHz, and 6 dBm at 1 GHz. Regardless of the clock frequency, a minimum clock amplitude of -6 dBm is recommended (per differential half-circuit input). At lower clock frequencies, particularly below 1 GHz, square wave clocks are suggested to achieve the desired slew rates without excessive clock amplitude.

Outputs

The outputs should be sensed differentially for the cleanest output waveforms. The output impedance is 50 Ohms resistive returned to the VccOB supply. The output stage is designed to drive 50 Ohms terminated to ground on each differential half-circuit output. The device offers a true ground-referenced common mode output that is typically within ±50 mV of ground; however it is possible to adjust the VccOB power supply slightly to fine-tune the output common-mode level to precisely 0V if desired. Additionally, the common-mode output level may be adjusted within the range of approximately ±0.5V by adjusting the VccOB power supply according to the approximate relation $Vocm=(VccOB-2)/2$ where Vocm is the output common mode voltage and VccOB can be varied in the range of +1 V < VccOB < +3 V.

Users operating at lower clock rates (such as < 1 GHz) may optimize their S/N ratio by filtering the output to a lower bandwidth than the output amplifier bandwidth of 7 GHz. Such an output filter will not reduce the sampled front-end noise (which is frozen into the signal samples and represents the majority of the THA noise because of the wide front-end bandwidth) but it can reduce the output amplifier noise contribution. The user can filter the output to the lowest bandwidth that still retains the maximum settling time required to support the chosen clock rate. Typically this optimal bandwidth is of the order of 2 - 3 times the clock rate. For example, a user operating at a clock rate of 350 MHz with a 1 GHz noise bandwidth output filter can achieve approximately 1 dB lower noise relative to the unfiltered output condition.

The output will have very sharp transitions at the clock edges due to the broad output amplifier bandwidth. The user should be aware that any significant length of cable between the chip output and the load will cause frequency response roll-off and dispersion that can produce low amplitude tails with relatively long time-constants in the settling of the output waveform into the load. This effect is most noticeable when operating in a lab setting with output cables of a few feet length, even with high quality cable. Output cables between the THA and the load should be of very high quality and 2 ft or less in length.

Reflections between the load and the device will also degrade the hold mode response. The output cable length can be adjusted to minimize the reflection perturbations to some extent. In general, the round trip transit time of the cable should be an integer number of clock periods to obtain the minimal reflection pertur-bation in the hold mode portion of the waveform. This cable length criterion essentially approximates a scenario where the low level double transit reflections time align with the output waveform sourcing them. The optimal performance is obtained when the THA is within 50 ps or less of the load since this gives a reflection duration equal to the approximate settling time of the device. In ADC applications the THA should be placed as close as possible to the ADC to minimize reflection effects on the path between the THA output and the input of the ADC.

3.0   *Track-and-Hold – Analog-to-Digital Converter Setup & Timing*

3.1   Track-and-Hold – Analog-to-Digital Converter Setup

A typical evaluation board laboratory setup using the HMC661LC4B as a master sampler for a high-speed ADC is shown in Figure 1. Synthesized generators with very low jitter must be used for input and clock signals to minimize jitter-induced noise floor degradation at high signal frequencies. 5% fractional bandwidth bandpass filters are used to clean up the signal sources by filtering non-harmonic spurious products and broadband noise which contributes jitter to the signal and clock sources. A broadband Picosecond Pulse Labs or equivalent phase splitter with 17 GHz bandwidth is used to convert the single-ended input signal to differential format. If desired, more conventional lower frequency baluns can be used for the clock, since it is limited to a much lower frequency. A variable delay line is used to properly time the ADC clock so that the ADC samples the settled hold-mode portion of the output waveform from the HMC661LC4B. DC blocking capacitors are used between the THA and the ADC for single-supply based ADCs since they operate at a non-zero common-mode input voltage bias level, usually provided internally. Alternatively, a DC coupled differential amplifier with variable output common-mode level can be used to match the DC levels of the HMC661LC4B and the ADC. The HMC661LC4B has a 0 V nominal common-mode output level but it can be adjusted over ± 0.5 V range if desired (see product data sheet for details).
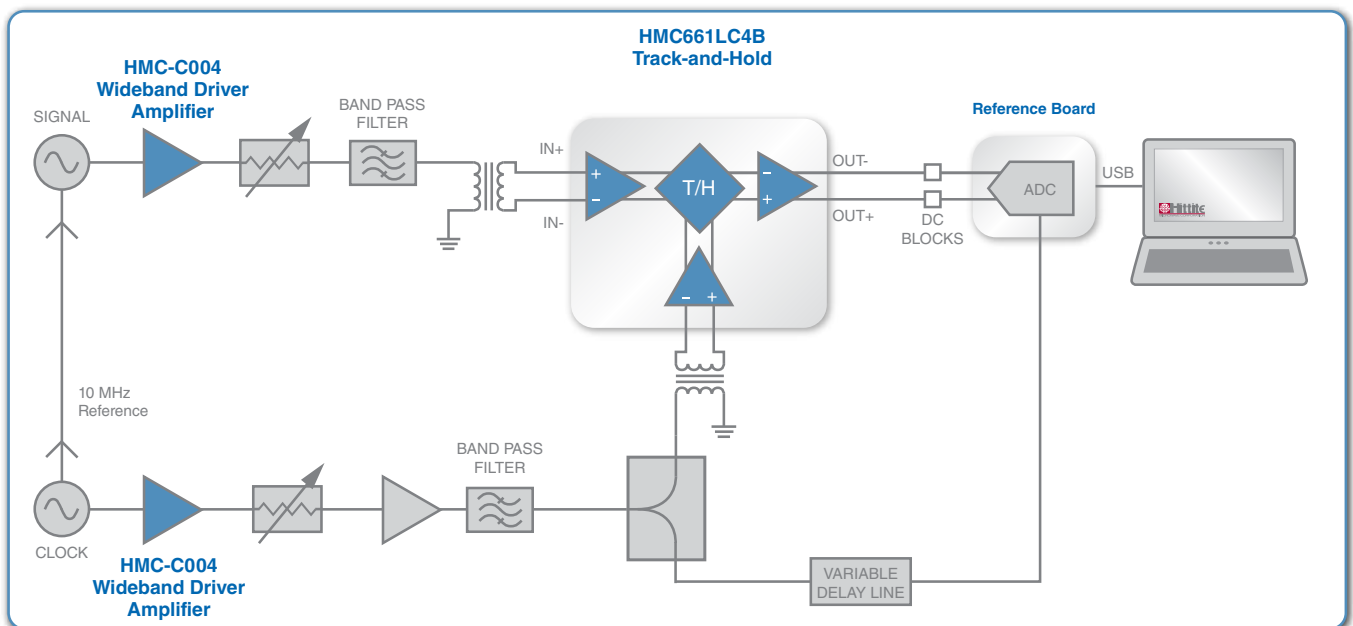

Figure 1. Block diagram of an A/D conversion assembly incorporating an HMC661LC4B T/H master sampler and an ADC evaluation board

As discussed previously, when using the HMC661LC4B in an actual system application, it is preferable to place the THA in close proximity to the ADC to minimize the transit time of reflection effects on the signal interconnect between the devices. This is best achieved by designing a custom board or hybrid that places the THA and ADC right next to each other. In that case, a fixed delay would be designed into the ADC clock signal path to obtain the proper timing of the ADC clock with respect to the THA output waveform. However, as we demonstrate here, a breadboard type setup with coaxial cable interconnects can provide accurate performance as long as the ADC clock is properly timed with respect to the THA clock.

Figure 2 shows a photograph of the breadboard setup. The differential outputs of the THA evaluation board are

connected to the DC blocks at the input of the ADC evaluation board via short SMA cables. At the two clock frequencies tested (1GS/s, 1.6 GS/s) the cable length is chosen such that the total transit time from the THA chip to the ADC chip is approximately an integer number of clock cycles to minimize the waveform perturbations arising from the double transit reflection effects described earlier.
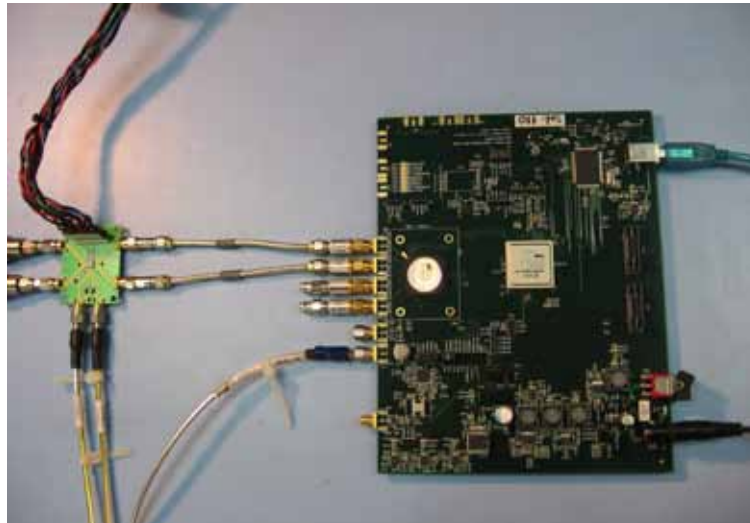

Figure 2. Breadboard Setup of the HMC661LC4B & ADC Evaluation Boards

3.2   Track-and-Hold – Analog-to-Digital Converter Timing

An important aspect of proper operation of the THA-ADC conversion assembly is establishing the correct timing of the ADC sampling with respect to the THA output waveform. This is referred to as the relative ADC clock delay. For proper operation, the ADC must sample the settled portion of the hold-mode output time segment in the THA output waveform. Although the assembly will function when the ADC is improperly timed to sample the THA track-mode output waveform segment, the proper bandwidth expansion will not be obtained because the ADC will simply be sampling a buffered (but not sampled) unity gain version of the input signal. In fact, the primary indicator that the ADC is properly sampling the hold-mode time segment is the extended bandwidth behavior. If the composite assembly shows a bandwidth more similar to the ADC input bandwidth, then in all likelihood, the timing is not properly adjusted and the ADC is sampling the track-mode portion of the THA output waveform.

The relative ADC clock delay can be calculated accurately if the various propagation delays of the board transmission lines, interconnects and the external cables are tabulated in addition to the internal group delays of the key paths inside the THA and the ADC. Table 2 shows the two key HMC661LC4B internal group delays that are relevant to the detailed computation of proper ADC clock timing: clock-to-hold-node delay and hold-node-to-output sample delay. The input signal to hold-node delay shown in the table is not a quantity that needs to be known for ADC clock timing calculations, but it is included here for information purposes. A key parameter also needed in this computation is the ADC aperture delay, defined as the difference between the clock delay to the ADC internal sample point and the signal delay to the ADC internal sample point. This aperture time, along with breadboard level interconnect delays, can often overshadow the small delays in the HMC661LC4B THA.

These calculations would typically be worthwhile or even necessary for a system implementation (although this would usually be easier than a breadboard setup since the interconnect delays would be much smaller). If the proper ADC clock delay (with respect to the THA clock) is determined and implemented accurately then the resulting assembly can be properly timed for all clock frequencies with only one ADC clock delay. If the proper delay is only implemented within a modulo clock period (i.e., proper phasing within a clock period but not the

minimum required delay), then the setting will be valid only for the specific clock frequency used. However, the detailed calculation and design of the necessary ADC clock delay is usually not necessary for laboratory breadboard setups since there is a simple algorithmic approach that can be performed with a variable delay line in the ADC clock path to rapidly arrive at the proper delay as described below.

Table 2. HMC661LC4B Internal Group Delays for Timing Calculations

Path	Group Delay (ps)
Signal input to hold-node	41.5
Clock input to hold-node	35
Output buffer delay from hold-node to output	43

An algorithmic approach to timing setup that utilizes a variable delay in the ADC clock path and the FFT output display of the ADC can be established. Before describing this procedure, it is helpful to understand how some of the key ADC output performance parameters depend on sampling position within the external HMC661LC4B THA waveform. Figure 3 shows the delay mapping of signal amplitude, SFDR, and noise spectral density as a function of the relative delay of the ADC clock (ADC sample point) with respect to the THA clock for the HMC661LC4B / ADC combination. The data shown in Figure 3 is taken for a 1GS/s sample rate. For reference, the approximate time locations of the HMC661LC4B output waveform track-to-hold transition (T-H) and the hold-to-track transition (H-T) are also indicated. The HMC661LC4B hold-mode is bound between these points while the track-mode time segment falls outside of the region bound by these points. This set of curves becomes very useful for understanding delay setup when the input frequency to the assembly is chosen well outside the bandwidth of the ADC. In Figure 3 the curves are plotted for an input signal frequency of 5 GHz which is well beyond the approximately 2.8 GHz bandwidth of the particular ADC.
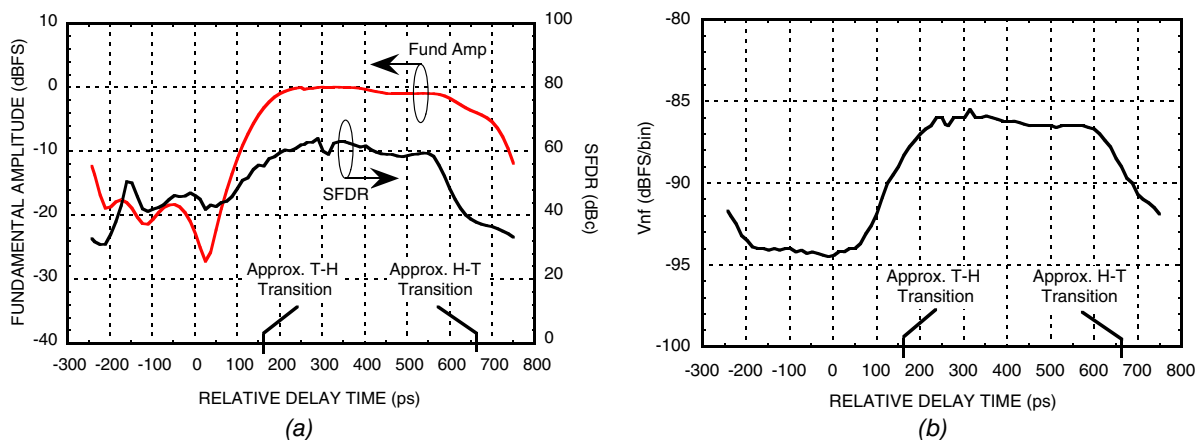

(a)

(b)

Figure 3. Delay Mapping of the Signal Amplitude, SFDR & Noise Spectral Density as a Function of Relative Clock Delay Between the ADC and the THA

    a) Delay mapping of fundamental amplitude and SFDR

    a) Delay mapping of the noise spectral density

The waveform presented to the internal sampler of the ADC is band limited by the input signal bandwidth of the ADC. The band-limiting within the ADC-internal front-end THA causes a substantial "rounding" of the sharp waveform transitions that are output from the HMC661LC4B. Hence, the delay mapping curves shown in Figure 3 also exhibit rounded transitions due to this ADC band-limiting. To first order, the -3 dB points of the amplitude curve correspond approximately to the time points of the T-H and H-T transitions of the HMC661LC4B output waveform.

From inspection of delay mapping curves like that shown in Figure 3 at a signal frequency beyond the ADC bandwidth but within the THA bandwidth, the following key behaviors can be deduced.

Signal Fundamental Amplitude

The bandwidth of the external THA is obtained when the ADC samples the hold-mode of the THA waveform. The lesser bandwidth of the ADC is obtained when the ADC samples the track-mode of the THA waveform. Samples in the transition regions can result in radical reductions in fundamental signal amplitude because the sample is not well defined at these points. This effect can be observed in the fundamental amplitude variation of Figure 3(a) where the amplitude near the transition points decreases significantly. In the track-mode region, the fundamental amplitude equilibrates at a constant level representative of the signal attenuation produced by the ADC input transfer function at that frequency.

Spurious Free Dynamic Range (SFDR)

SFDR is relatively constant for ADC samples within the majority of the hold-mode region of the THA waveform. It is preferable to ensure that the samples are taken near the end of the hold-mode where the waveform is well settled, but before the H-T transition rounding region caused by the ADC band-limiting. As the clock frequency increases, it becomes more important to optimize the position of the samples in the hold-mode time segment to achieve maximum SFDR. For the ADC measured, a reasonable ADC sampling time is about 120 ps advanced (earlier in time) with respect to the H-T transition point. SFDR decreases rapidly when the ADC sample point gets into the H-T transition region because the signal sample is not well defined at these transition points.

Noise

Figure 3(b) shows that the noise spectral density increases when the ADC samples are taken in the hold-mode waveform segment relative to those taken in the track-mode segment. This increase can also be observed in the total integrated time domain noise as well. This is expected theoretically and it occurs because ADC samples in the hold-mode region reflect the sampling of the HMC661LC4B over the full 18 GHz input bandwidth. From a frequency domain standpoint, the sampling process folds the noise over this entire bandwidth into the much lower bandwidth of one Nyquist interval. From a time domain standpoint this effect can be viewed as the instantaneous front-end noise being effectively "frozen" into the samples at the instant of sampling. This increases the noise spectral density in the first Nyquist interval which is fully detected by the ADC because it falls within its input bandwidth. On the other hand, samples in the track-mode region do not reflect sampling by the HMC661LC4B. The noise spectrum still occurs over 18 GHz of bandwidth but the ADC never "sees" the HMC661LC4B sampling and there is no folding effect for the ADC samples in the track-mode portion of the waveform. The majority of this spectral noise falls outside of the bandwidth of the ADC, reducing the total noise detected.

In summary, the input noise bandwidth is 18 GHz for ADC samples in the hold-mode region of the HMC661LC4B output waveform while the input noise bandwidth is the ADC input bandwidth for ADC samples in the track-mode of the HMC661LC4B. For example, it is not unusual to observe an 8 to 10 dB difference between the noise levels of the hold-mode and track mode ADC samples for the 2 to 3 GHz input bandwidths of typical high speed converters. This is expected because the ratio of the bandwidths is also approximately 8 to 10 dB. This makes the relative noise level a useful parameter to indicate the timing region of the ADC samples.

3.3   Simple Track-and-Hold - Analog-to-Digital Clock Timing Procedure for Breadboard Setups

Utilizing the characteristics described above, a straight forward approach can be established for determining ADC clock timing and optimization in a typical breadboard setup. This procedure uses a variable delay in the

ADC clock path and the information provided by the FFT spectrum of the ADC. The steps to this approach are:

1) Setup the THA-ADC timing with arbitrary ADC clock delay and a variable delay.

Setup the THA-ADC timing initially with arbitrary ADC clock delay (no need for detailed calculations) and a variable delay, with respect to the THA clock. The variable delay should allow adjustment over at least half of a clock cycle. Place the initial position of the delay in the center of its delay range. Due to the fixed pedestal delay of most trombone type variable delay lines, it can be helpful to use identical variable delays in both the THA clock and the ADC clock paths so that the fixed pedestal delay is balanced in both paths. This is extremely helpful when setting the exact ADC clock delay for clock frequency independent timing where no excess modulo clock period delay can be tolerated. The relative ADC delay can then be adjusted by either or both delay lines. Balanced length cables should be used in the HMC661LC4B clock path between the balun and the clock inputs if the clock is driven differentially.

2) Apply an input signal near full scale outside the bandwidth of the ADC but within the bandwidth of the THA.

Apply an input signal at a level just beneath ADC full scale, at a frequency which is well beyond the ADC input bandwidth but within the HMC661LC4B THA bandwidth. A frequency of 5 GHz is a good choice for converters with 2-3 GHz input bandwidth.

3) Observe the FFT spectrum and identify the first order beat product (fundamental).

Power up the devices, observing an FFT spectrum display of the ADC output and identify the first order beat product resulting from heterodyning the input signal with the clock harmonic that places the resultant beat product in the first Nyquist interval. This is the fundamental of interest which is representative of the converted signal amplitude. Example: for a clock frequency of 1 GHz and an input signal frequency of 5.049 GHz, the down-converted first order beat product is at 5.049-5(1)=49 MHz

4) Determine whether the ADC sample is occurring in the track-mode or hold-mode region of the external THA output waveform.

This is accomplished by observing the fundamental amplitude. If a signal close to full scale is obtained, then the ADC clock timing is sampling the hold-mode waveform segment and the assembly is exhibiting the expanded bandwidth of the HMC661LC4B. If the signal amplitude observed is representative of the transfer function attenuation that would be obtained from the ADC input bandwidth at that frequency, then the ADC is sampling the track-mode waveform segment and exhibiting the reduced bandwidth of the ADC. If there is uncertainty in the status of the fundamental amplitude then mapping the amplitude and noise of a few different delay points initially over a small delay range (like ± 50 ps) can rapidly help assess if the ADC sample point is sitting on a T-H or H-T transition. If this is the case then shift the delay to avoid the transition region so that the samples land squarely in either the track-mode or hold-mode regions. In addition, mapping a few amplitude and noise points spread over a half clock cycle can rapidly assist in determining the operating regime and the location of transitions.

5) Set the THA clock polarity to place the ADC samples in the hold-mode of the HMC661LC4B.

If the ADC is sampling the hold-mode in step 4 above, then the phasing of the THA clock connections can be left alone. If the ADC is sampling the track-mode then the differential clock connections to the THA should be reversed to shift the relative sampling delay between the THA and ADC by one half-clock cycle. This change should place the ADC sample point in the hold-mode waveform segment. If the amplitude does not increase to near full scale after shifting the clock phase to the THA, then vary the ADC clock delay by small amounts while monitoring to assess if the ADC samples happen to be sitting on a transition point.

6) Identify the H-T transition and set the ADC sample point optimally advanced with respect to this point.

Once the ADC samples are known to be in the hold-mode, map a few points with increasing ADC clock delay until the location of the H-T transition is determined. To first order, this should occur at about the

-3 dB point of the delay mapping amplitude curve. Once the H-T transition is identified, the ADC sample point can be advanced in time with respect to this transition until the amplitude and SFDR performance reach relatively equilibrated values. This will typically occur 30 to 150 ps advanced with respect to the H-T transition, depending on the input bandwidth of the ADC and the resulting amount of band limiting "rounding" of the transition. This point represents an acceptable point for the ADC sample timing. If the ADC relative delay has been set to the absolute minimum (no excess modulo clock period delay) then the timing should be valid for all clock frequencies. If the ADC relative delay has only been properly phased but contains excess modulo clock period delay, then the timing procedure will need to be redone if the clock frequency changes.

4.0   Summary

This application note discusses the HMC661LC4B Ultra wideband THA and its application as a master sampler for bandwidth and linearity enhancement in high speed ADCs. Guidelines for interfacing the HMC661LC4B to ADCs are presented and a simple systematic approach for establishing proper ADC sample time/clock timing in a breadboard setup is provided.

Examples of the performance that can be obtained when the HMC661LC4B is used in an evaluation board setup with some current high speed ADCs may be found in the companion Hittite application note: *Bandwidth & Performance Improvements of High Speed A/D Converters Using the HMC661LC4B.*